micralyne

Multi-layer Silicon MEMS Processes and Devices

Detailed MEMS Examples for Smart Systems

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Outline

- Micralyne Introduction
- MEMS in Optical Telecom Smart Systems
- Variable Optical Attenuator (VOA)
- VOA MEMS Fabrication Method
- MEMS Sensors for Smart Automotive and Medical Imaging Systems
- Capacitive Micro-machined Ultrasonic Transducer (CMUT) Fabrication
- Summary

Goal: To provide a the audience with a component level view of two example of MEMS devices used in smart systems.

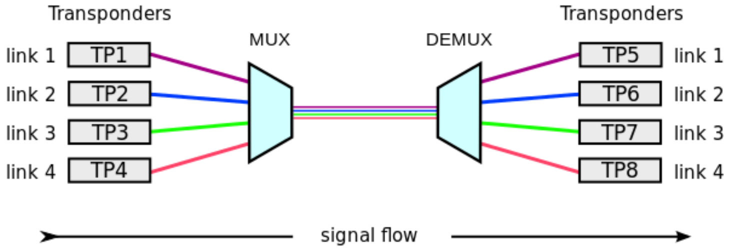
Micralyne Introduction

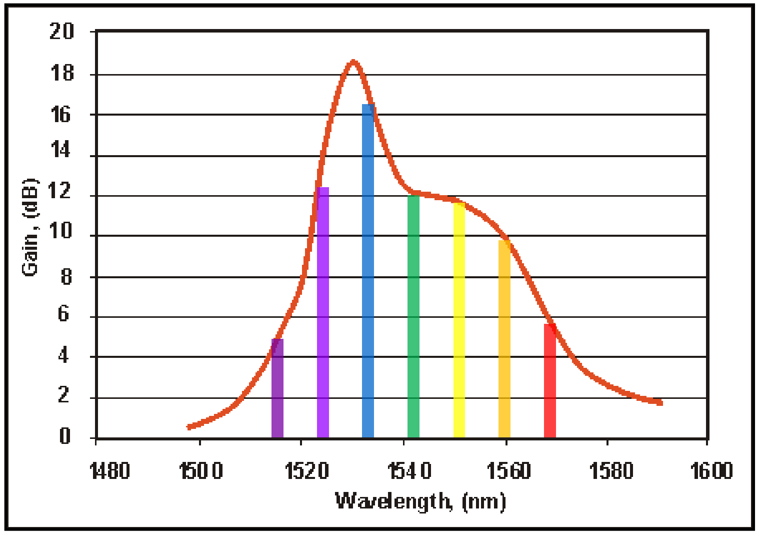
- A top independent MEMS provider
- Located in Edmonton, Alberta, Canada
- Founded in 1982 and privatized in 1998
- 55,000 sq ft. (5000 m^2) MEMS facility
- Sensors, Optical, Medical, and other MEMS devices
- Sales in Japan since 2004, Adamant partnership
- Development and Manufacturing of Complex MEMS

Smart Optical Communication Systems

- Stable fiber optic communication requires management of multiple wavelengths of light to fully utilize fiber capacity.
- Attenuation during transmission and amplification to not occur uniformly over all wavelengths.
- Other functions such a remote power control and wavelength switching are also needed within the network.

Wavelength Division Multiplexing (WDM)

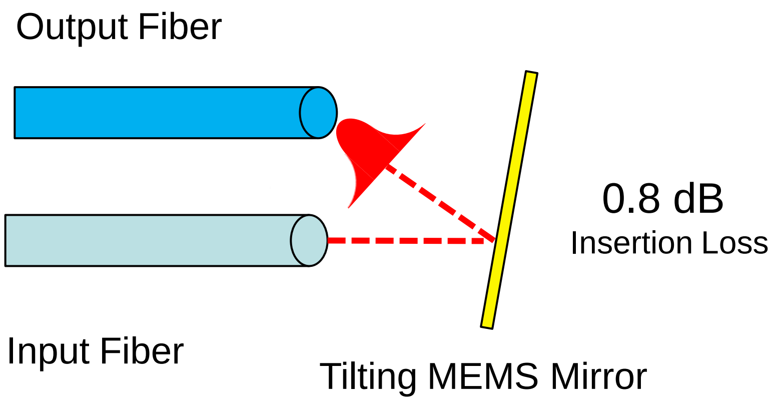




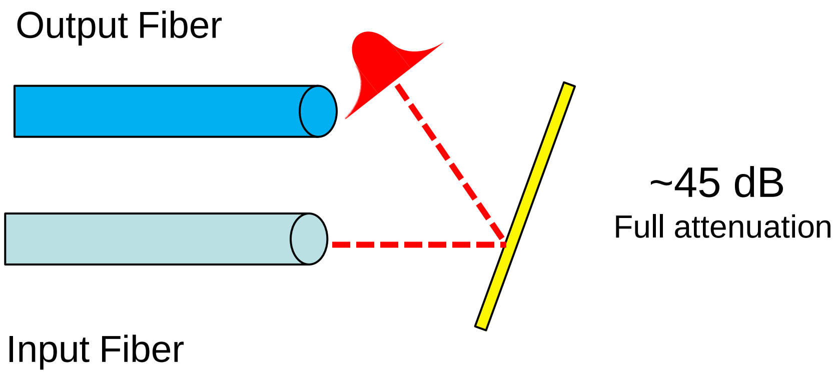
Erbium Doped Fiber Amplifier Gain

Variable Optical Attenuator (VOA)

- Network component that can be used for wavelength management (one VOA per channel), on/off switching, or whole signal attenuation.
- MEMS mirror can operate in the range from 0 to 20 volts depending on the MEMS and system design. Typically 0 to 20V and 0 to 5V versions.

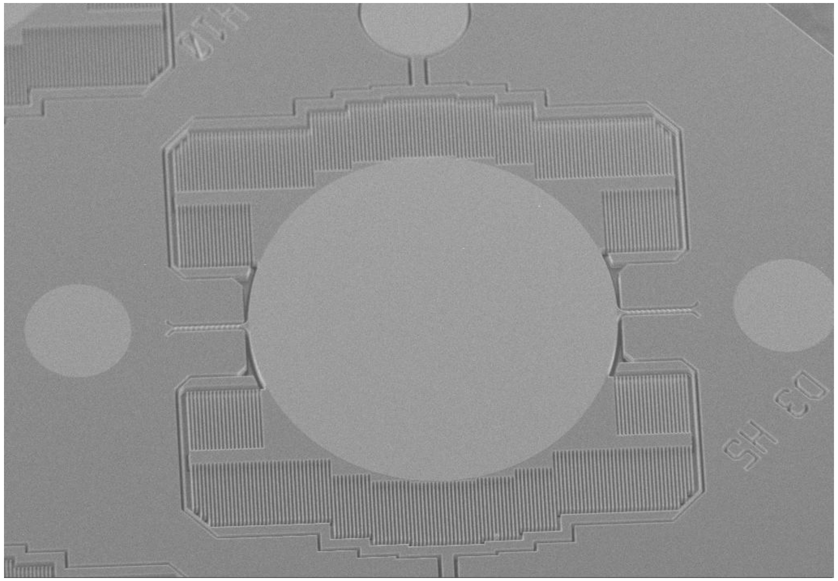


Low Attenuation

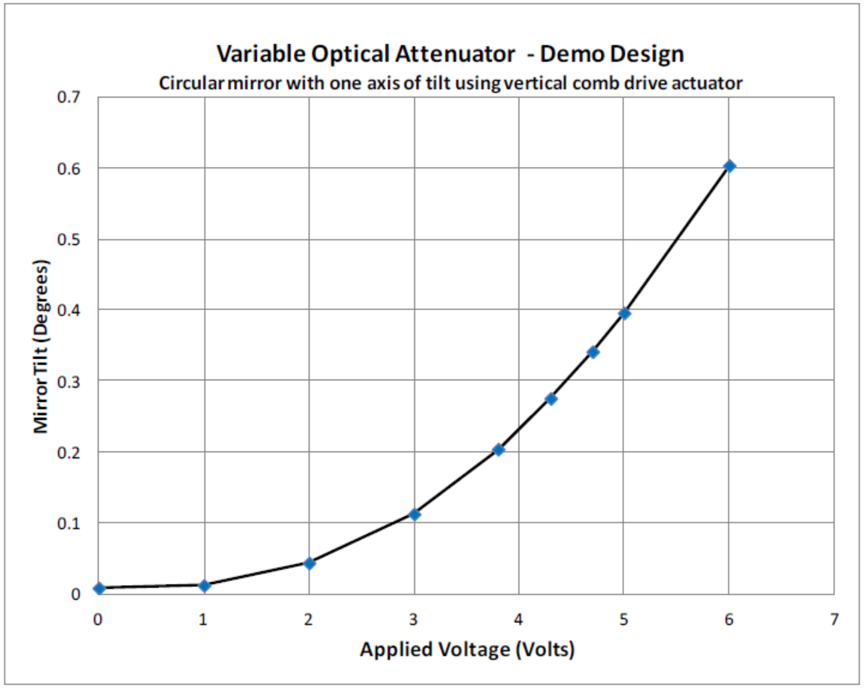


High Attenuation

VOA MEMS Example



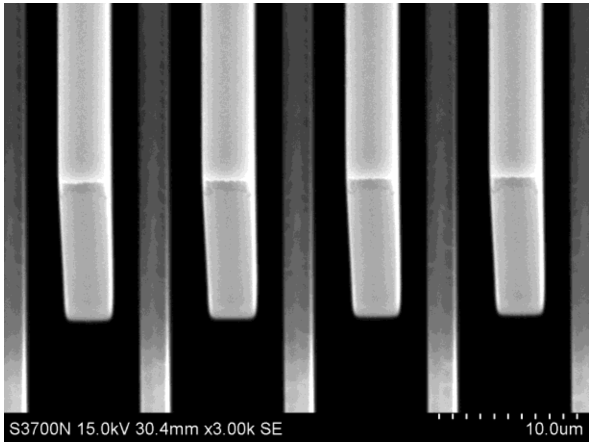
VOA MEMS Mirror



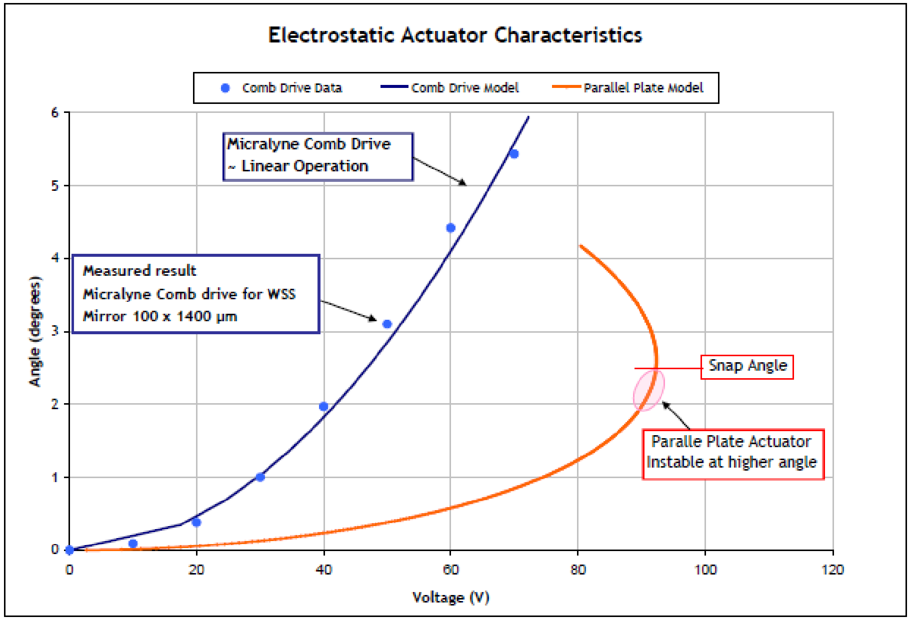
Voltage vs. Tilt Characteristics

Vertical Comb Drive Actuator

- Uses electro-static force to tilt mirror on a silicon torsional hinge
- Vertical comb drives:
  - » are more efficient than parallel plate actuators
  - » provide better actuation characteristics than simple parallel plate actuators

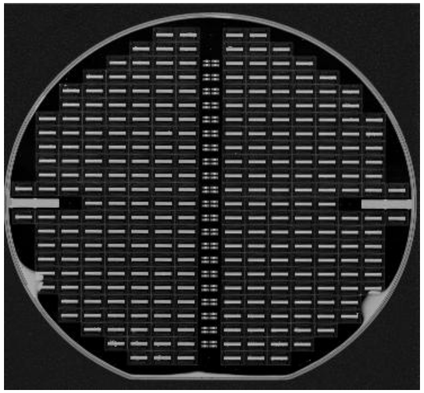


Comb Drive Ends

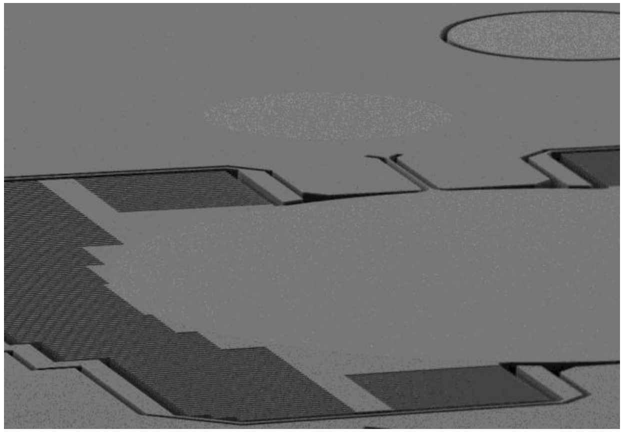


Key Process Technologies

- Deep Reactive Ion Etching for high aspect ratio bulk machining of silicon
  - Multi-height structure defined in single layer of silicon
  - Top surface remains bondable
- Aligned wafer Si-Si fusion bonding
- Stepper lithography
  - Non-contact for low defect count. Alignment of out-of-plane layers to within 0.4 µm
- Low stress metallization (TiW/Au)
  - Enables metalized membranes with low stress



Acoustic image of bonded wafer



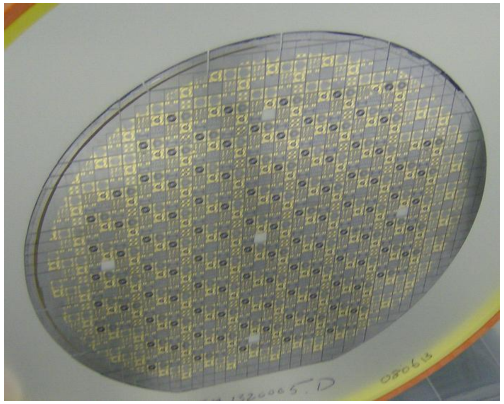
Mirror with better than 1.5 m ROC

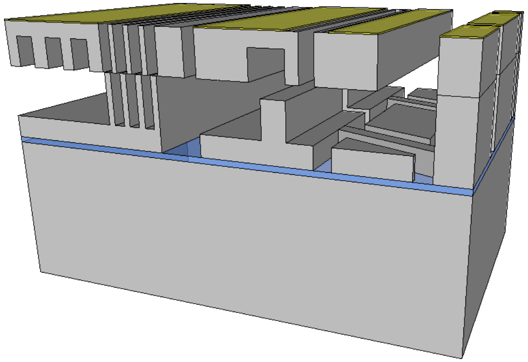
MicraGEM-Si™ MEMS Process Flow

- VOAs can be made with the following process

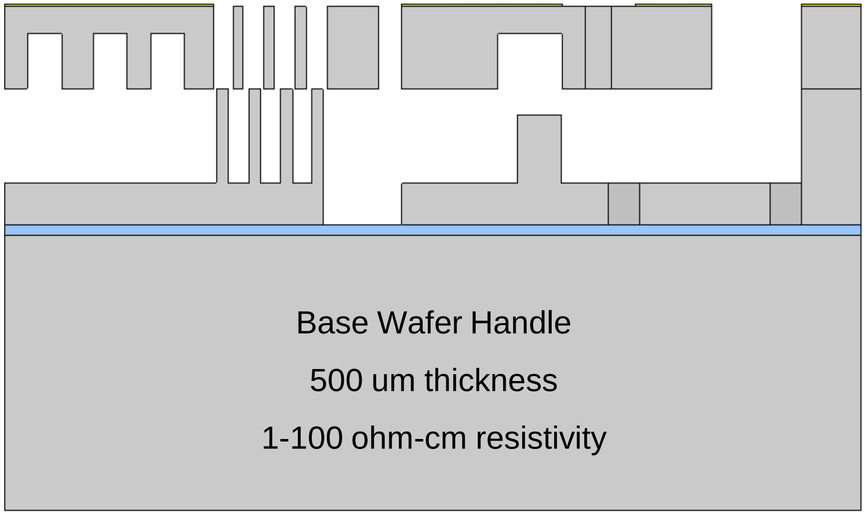
- MicraGEM-Si™ is a silicon-on-insulator based MEMS process for devices such as micro mirrors, optical switches, resonators, inertial and bio sensors

- The technology includes:
  - Two thick SOI structure layers with bulk micromachining
  - Deep etch features on the upper and lower devices layers are aligned with sufficient accuracy to enable vertical comb drive structures
  - Upper and lower devices layers are connected electrically through the bond interface allowing 3D routing of electrical signals
  - Low stress gold metallization on the top surface is suited for highly reflective mirrors as well as contact pads for gold wire bonding





Process Overview - Generalized Cross-Section



Top Wafer Device Layer, 30 µm

0.01-0.02 ohm-cm

Base Wafer Device Layer, 50 µm

0.01-0.02 ohm-cm

Z – Top Wafer Frontside

Y – Top Wafer Backside

B – Base Wafer Device Layer

Light Blue – Oxide

Grey – Silicon

Yellow – Lowstress metal

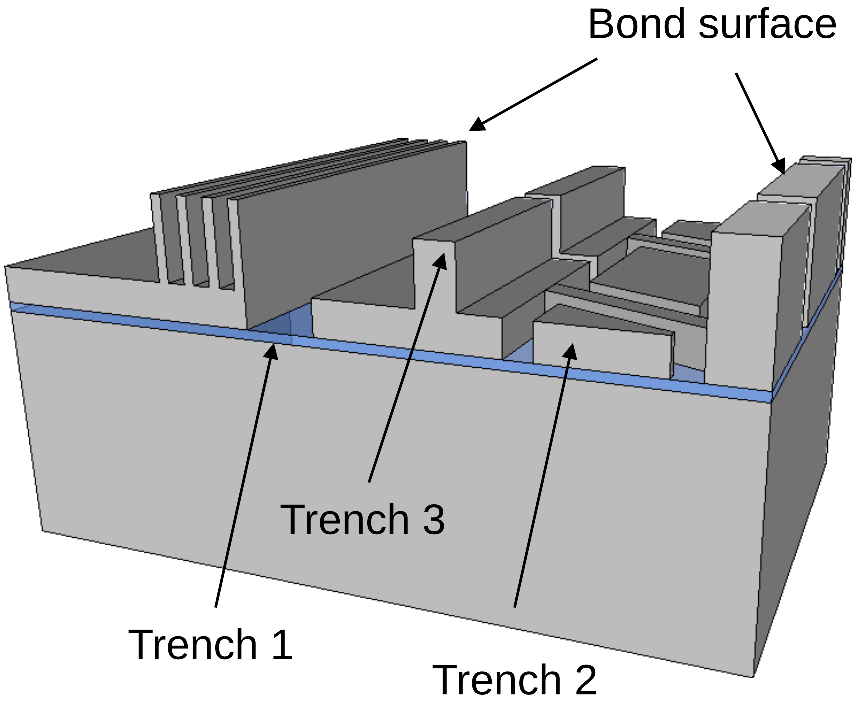
A – Base Wafer Backside

Major Process Steps

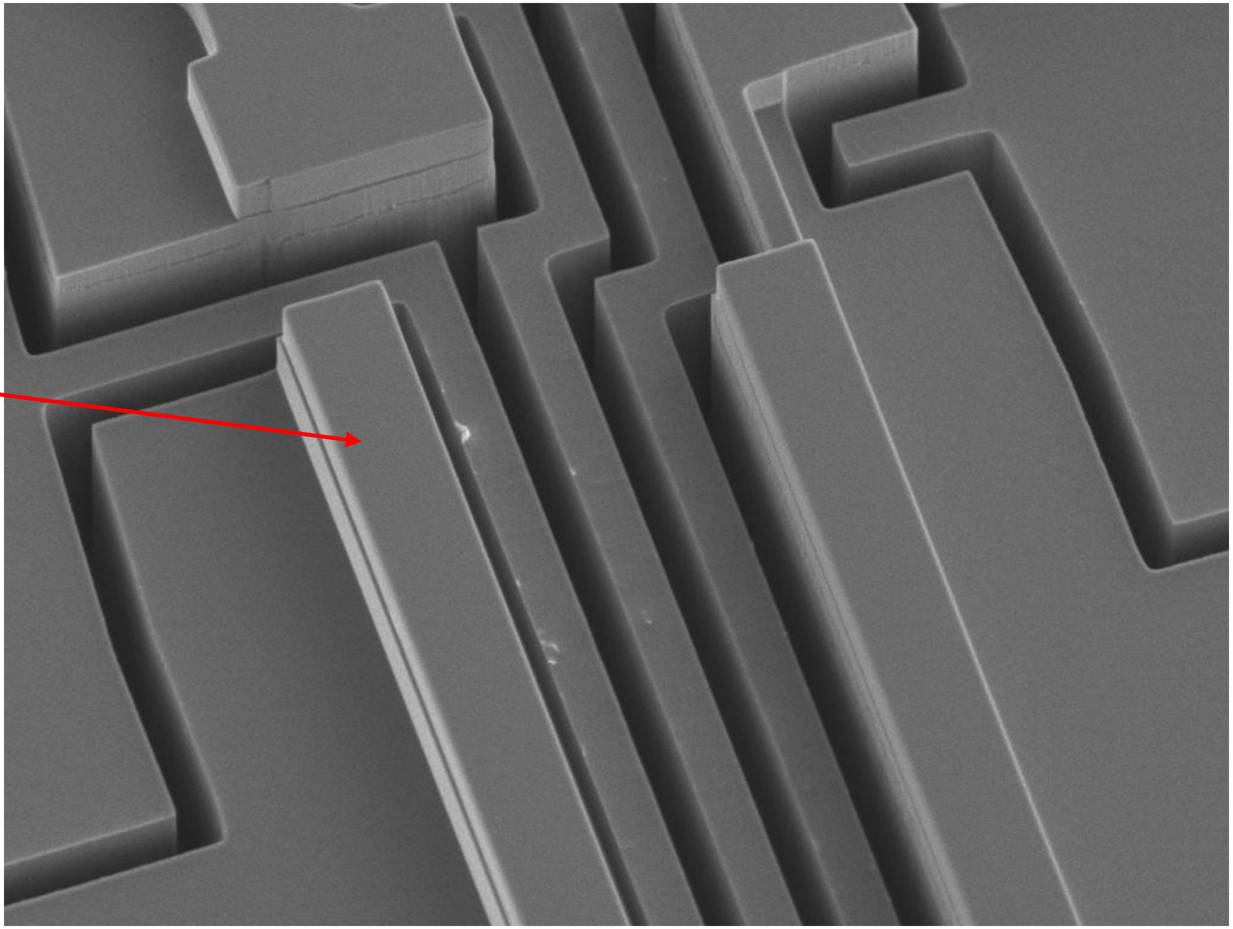
- Step 1 – Define and etch silicon structure in the Base Wafer device layer (B)
- Step 2 – Define and etch Top Wafer backside (Y)
- Step 3 – Bond Base Wafer to Top Wafer
- Step 4 – Remove Top SOI handle and buried oxide
- Step 5 – Deposit low stress metal on Top Wafer fronside (Z), pattern metal
- Step 6 – Pattern and etch Top Wafer device layer to release structures
- Step 7 – Dicing

Step 1 – Pattern and Etch Base Wafer

- Define Trench 1, Trench 2 and Trench 3 regions
  - » Trench 1 – regions etched 50 µm, all the way to the buried oxide
  - » Trench 2 – regions etched 35 +/- 2 µm, leaving a 15 µm silicon feature on the buried oxide
  - » Trench 3 – regions etched 10 +/- 1 µm , leaving a 40 µm silicon feature on the buried oxide



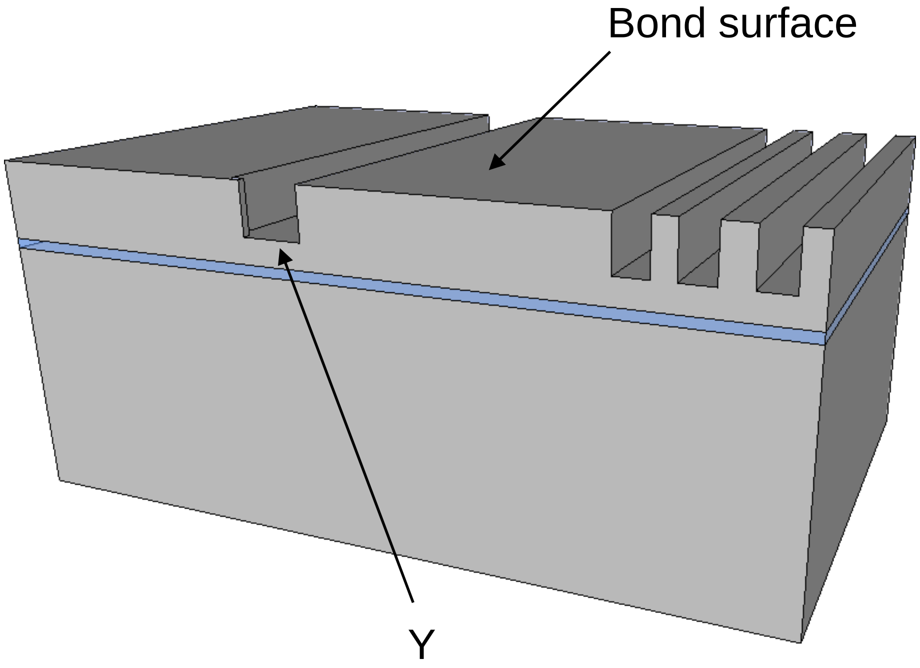
Multi-layer Etched Base Wafer



Bond surface

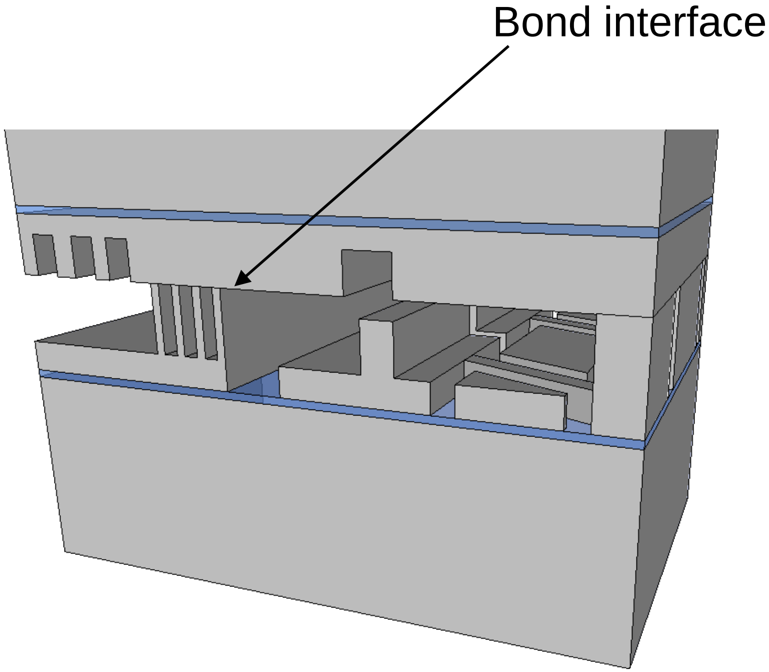
Step 2 – Define and Etch Top SOI Wafer Backside

- Define Top SOI Wafer Backside etch
  - Etch depth is 20 +/- 1 µm
  - Min feature is 1.5 µm line, 1.5 µm space
  - In the final structure, the regions etched here will be left as a 10 µm membrane



Step 3 – Bond Base Wafer to Top Wafer

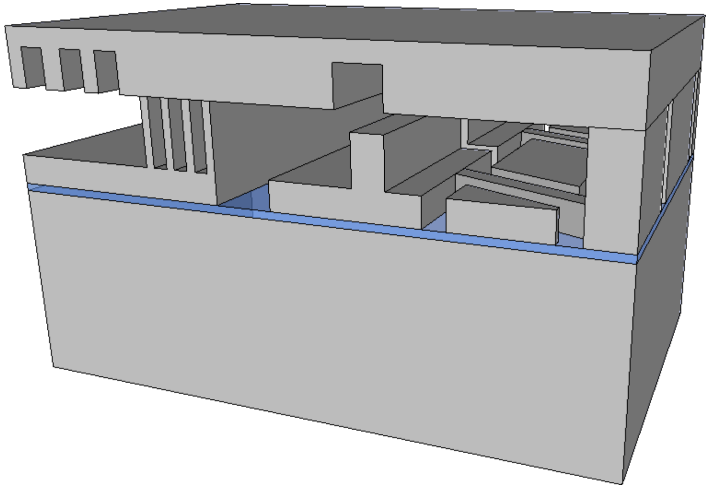
- Bottom and Top Wafers are aligned and fusion bonded in a controlled environment (under vacuum)
  - » Post bond alignment accuracy is +/- 10 µm
  - » The bond is mechanical, but also provides electrical connection between the two layers of silicon



Bond accuracy is +/- 10 µm

Step 4 – Remove Top SOI Handle and Buried Oxide

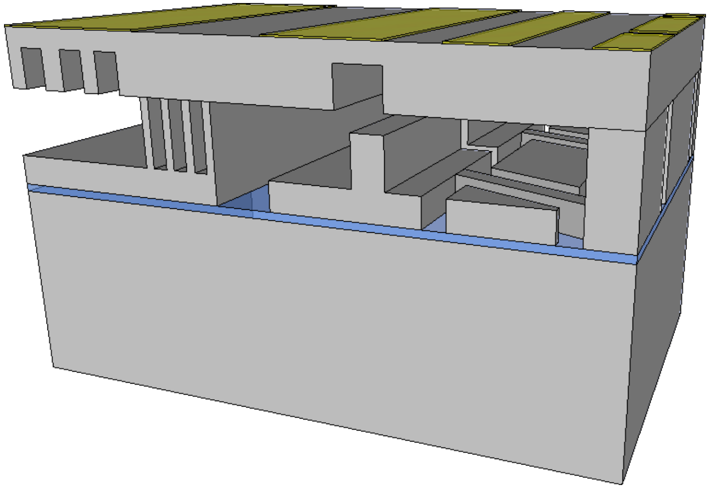
- The Top Wafer SOI handle is removed with a grind and polish process
- The exposed buried oxide is stripped leaving a pristine optically flat silicon surface



Step 5 – Deposit and Define Metal

- The top device layer is blanket coated with a low stress TiW/Au metallization. The residual metal stress is 40-140 MPa.

- The metal is then patterned to form device elements such as electrodes, bond pads and highly reflective surfaces. This is also the recommended layer to put labels.



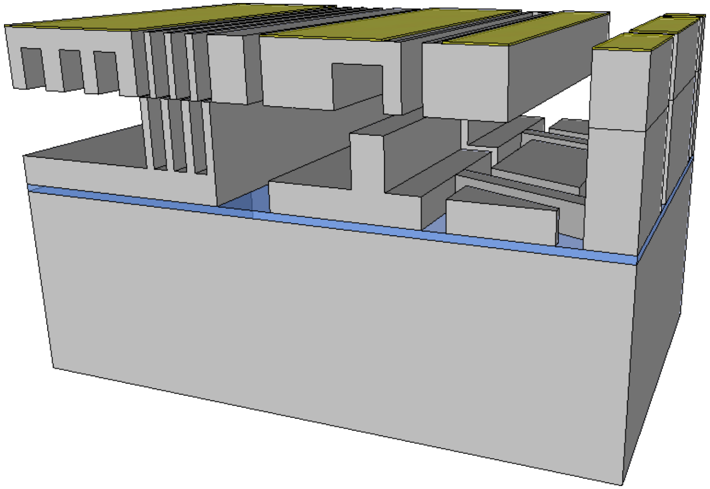
Step 6 – Release Patterning and Etching

- The final DRIE process etches completely through the 30 µm thick Top device layer and releases the MEMS structures

- During this process, features in the lower layers will be exposed to over-etching when the etch breaks through and before all features are etched to completion. In general, very wide features will open first, while high aspect ratio features will open last.

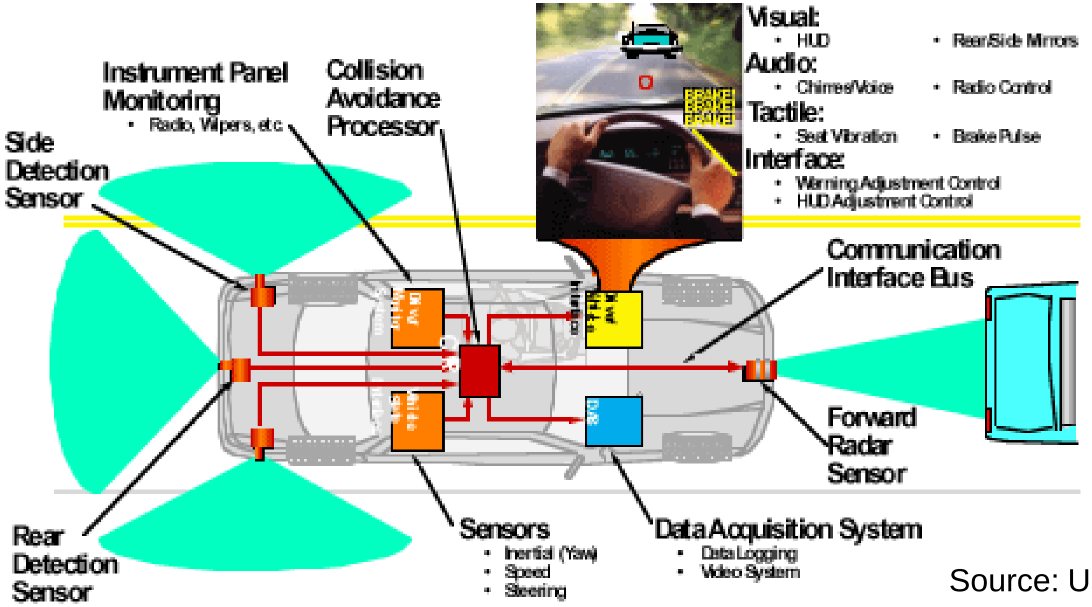
- The accuracy of this pattern is with 0.4 µm of the base device layer pattern

- Step 7: Dicing



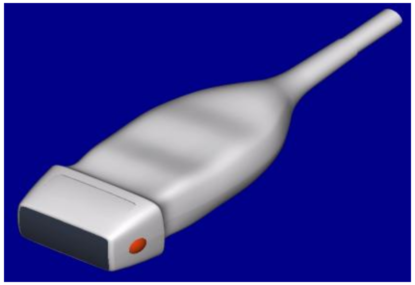
MEMS Sensors for Smart Automobile Systems

- A variety of technologies are available for sensing the surroundings of vehicles to allow autonomous driving (adaptive cruise control, park assist) and increased safety (lane change warnings, crash avoidance).
- Safety regulation has accelerated the progress of these systems.
  - » CMUT devices made using MEMS technology and will offer multi-frequency arrays as well as superior acoustic coupling.



Source: US Government http://www.nhtsa.gov

Sensors for Medical Imaging

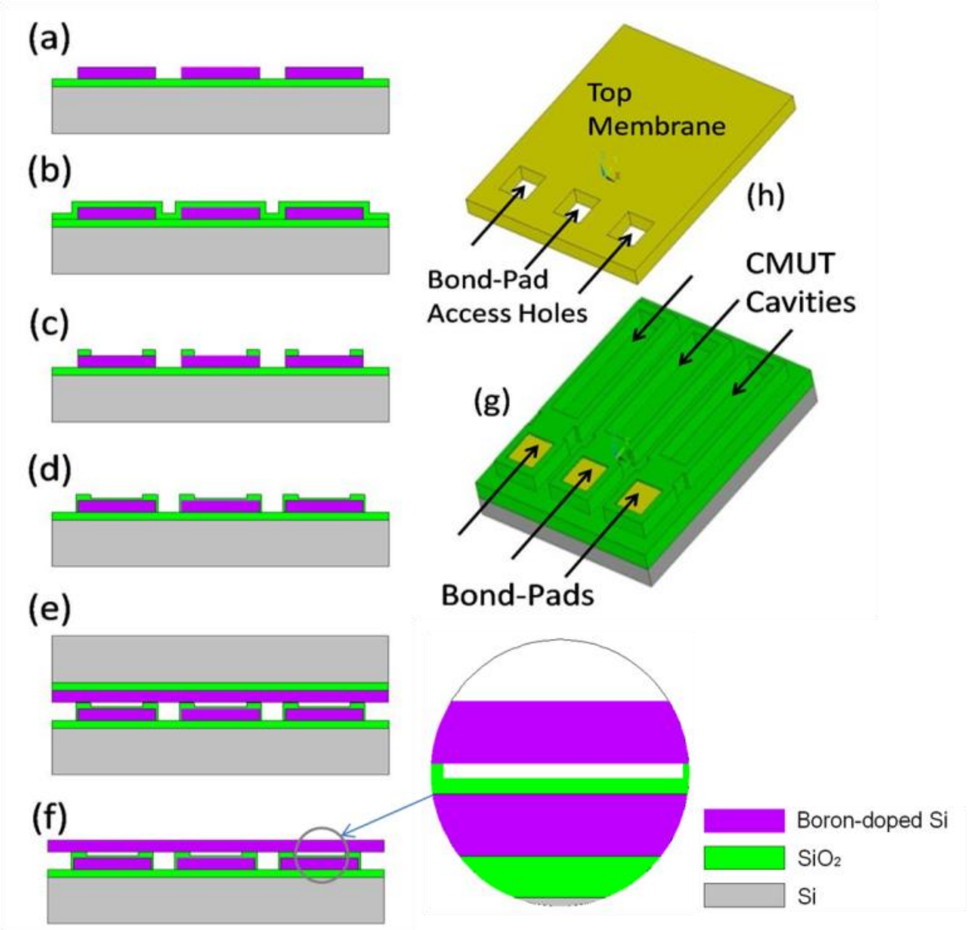


- Presently 2D images are made by clinical operators moving a hand held wand containing one linear array of piezoelectric ultrasonic transducers over the surface of the patient and one frequency is used.
- Capacitive Micro-machined Ultrasonic Transducers (CMUT) offer the ability to use multiple frequencies and a 2D array of elements to image higher resolution and in three dimensions.
  - » This gives the ability to move from crude images to real time topographical images.

Capacitive Micro-machined Ultrasound Transducers

CMUT technology offers many potential advantages over traditional linear array piezoelectric transducer technology, including:

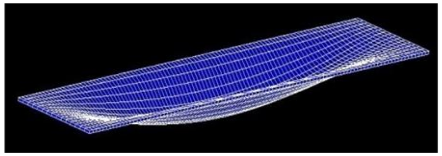
- Advantages of wafer fabrication scale
- 2D arrays offer higher resolution
- Greater sensitivity
- Superior acoustic impedance matching
- Potential to co-integrate with electronics
- Choice of frequencies of interest possible with just a change in geometry



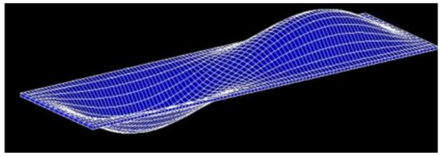
Bonded double SOI process cross section - three devices

CMUT Systems

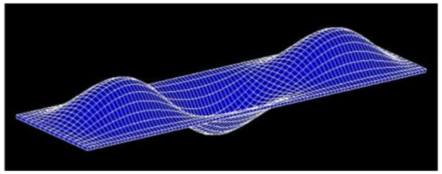
- CMUT technology provides MHz sound wave generation and detection
- Predictive modeling algorithms to design for specific frequencies
- CMUT devices allow for a simpler interface with drive electronics compared to piezoelectric transducers
- Electronic and acoustic testing have verified model results



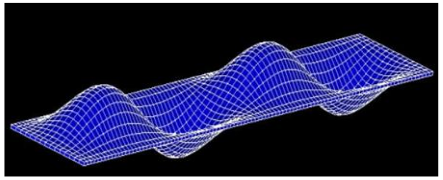
(a) First modal



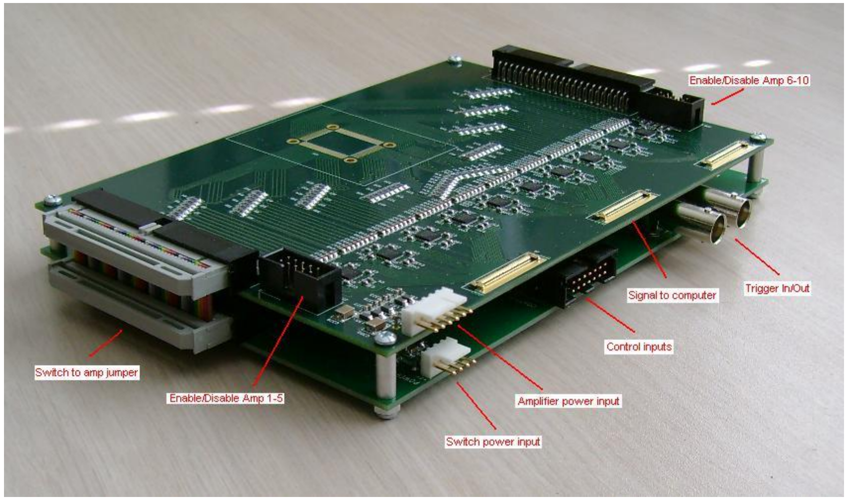
(b) Second modal



(c) Third modal



(d) Fourth modal



Model outputs and test systems used with Micralyne's academic development partner.

Summary

- Two important Smart Systems MEMS devices were presented.
- Both can be fabricated with different versions of a multi-layer silicon process flow.
- MEMS components are a key element in the design of smart systems, because they sense and interact with the world around us.

Thank you

Questions?

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